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(54) Image information transmitting system.

(57) In an image information transmitting system of this invention, an image information signal constituted by a plurality of data constituting one frame is input. A plurality of pixel data blocks each consisting of a predetermined number of pixel data are formed from the input image information signal. Dynamic range information data associated with dynamic ranges of values of the pixel data constituting each pixel data block are formed in units of the plurality of pixel blocks. The pixel data constituting the pixel data block is coded using the dynamic range information data to form a plurality of coded data in units of pixel data blocks. The dynamic range information data and the coded data are sent onto a transmission line. These transmitted data are received, and a data portion of the dynamic range information data and the coded data which has an error is interpolated. High-quality image information can be efficiently transmitted.

FIG. 7A

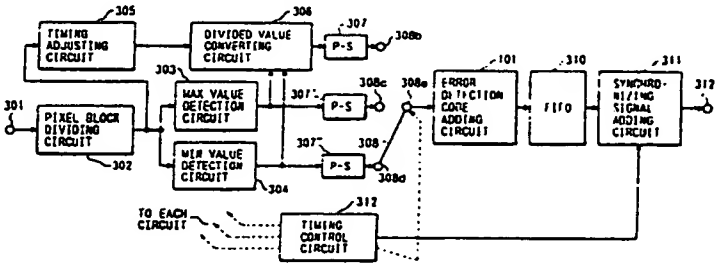


FIG. 7B

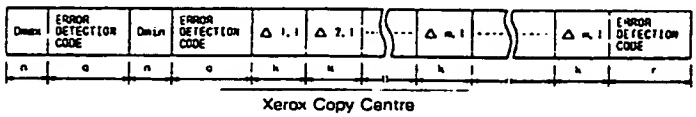


IMAGE INFORMATION TRANSMITTING SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image information transmitting system and, more particularly, to an image information transmitting system capable of performing high-efficiency coding.

Related Background Art

For example, a high-efficiency coding scheme for a television signal is known as an image information transmitting scheme of this type. In this high-efficiency coding scheme for the television signal, since a transmission band must be narrowed, a so-called MIN-MAX method for reducing the average number of bits per pixel is employed. The MIN-MAX method will be described below.

A television signal has strong correlation with time in a space. When an image is divided into small blocks, the blocks often have only a small dynamic range due to local correlation. A local dynamic range is obtained in each block, and adaptive coding is performed to perform highly efficient data compression.

This coding scheme will be described in detail with reference to the accompanying drawings.

Fig. 1 is a schematic block diagram of an image information transmitting system as a prior art. The image information transmitting system includes an input terminal 301. An analog signal obtained by raster-scanning, e.g., a television signal is sampled at a predetermined frequency, and data (n bits/sample) is input to the input terminal 301. The digital image data having 2^n gradation levels are supplied to a pixel block dividing circuit 302.

Fig. 2 is a view showing a state wherein one-frame pixel data are divided into pixel blocks. In the pixel block dividing circuit 302, the one-frame pixel data are temporarily stored in a memory or the like. As shown in Fig. 2, the pixel data are read out in units of blocks each having (ℓ x m) pixels, i.e., ℓ pixels in the horizontal direction (to be referred to as an H direction hereinafter) and m pixels in the vertical direction (to be referred to as a V direction thereinafter). That is, the data are output in units of pixel blocks.

Fig. 3 shows a format of each pixel block. This pixel block contains pixel data $D_{1,1}$ to $D_{m,\ell}$. Image data output from the pixel block dividing circuit 302 are input to a MAX value detection circuit 303, a MIN value detection circuit 304, and a timing adjusting circuit 305. Of all the pixel data ($D_{1,1}$ to $D_{m,\ell}$) in each pixel block, a pixel (D_{max}) having a MAX value and a pixel (D_{min}) having a MIN value are detected by and output from the detection circuits 303 and 304, respectively.

The timing adjusting circuit 305 delays all the pixel data by a period required to cause the MAX and MIN value detection circuits 303 and 304 to detect the pixels D_{max} and D_{min}. The pixel data are sent to a divided value converting circuit 306 in units of pixel blocks in a predetermined order. For example, data are sent in an order of $D_{1,1}$, $D_{2,1}$, $D_{3,1}$,..., $D_{m,1}$, $D_{1,2}$,... $D_{m,2}$,..., $D_{1,(\ell-1)}$,... $D_{m,(\ell-1)}$, $D_{1,\ell}$,..., and $D_{m,\ell}$ in units of pixel blocks.

All the pixel data ($D_{1,1}$ to $D_{m,\ell}$) and MAX and MIN values (D_{max} and D_{min}) of each pixel block are input to the divided value converting circuit 306 and are compared with 2^k (where k is an integer smaller than n) quantization levels between the values D_{max} and D_{min}, thereby obtaining k-bit division codes ($\Delta_{1,1}$ to $\Delta_{m,\ell}$). The quantization state is shown in Fig. 4A.

As shown in Fig. 4A, the division code $\Delta_{i,j}$ is output as a k-bit binary code. The obtained k-bit division code $\Delta_{i,j}$ and the n-bit values D_{max} and D_{min} are converted into serial data by parallel-to-serial (P-S) converters 307, 307', and 307", respectively. One of the outputs from the P-S converters is selected by a data selector 308, thus obtaining serial data shown in Fig. 5A. The data output from the data selector 308 is added with a p-bit error correction code (Fig. 5B) by an error correction code adding circuit 309. The output from the error correction code adding circuit 309 is processed by a first-in first-out (FIFO) memory 310 along the time axis so as to obtain a predetermined data transmission rate. In addition, an output from the FIFO memory 310 is added with a synchronizing signal by a synchronizing signal adding circuit 311. The obtained signal is sent out from an output terminal 312 onto a transmission line (a magnetic recording-reproducing system such as a VTR).

The synchronizing signal is added in units of pixel blocks or every plurality of pixel blocks. The operation timings of the above circuits are determined on the basis of timing signals output from a timing control circuit 313.

Fig. 6 is a block diagram showing a schematic arrangement of a receiving side corresponding to a data transmitting side shown in Fig. 1. The receiving side in Fig. 6 includes an input terminal 821 for receiving transmission data highly efficiently coded at the transmitting side. The input transmission signal is supplied to a synchronizing signal sepa-

rating circuit 822 and an error correction circuit 823.

The synchronizing signal separating circuit 822 separates a synchronizing signal from the input transmission data and sends the separated synchronizing signal to the error correction circuit 823 and a timing control circuit 831.

The error correction circuit 823 separates the error correction code from the transmission data in synchronism with the synchronizing signal supplied from the synchronizing signal separating circuit 822, detects a data error generated along the transmission line in accordance with the error correction code, corrects this error, and supplies the corrected data to a data selector 824.

The timing control circuit 831 controls operating timings of the respective circuits on the receiving side on the basis of the synchronizing signal supplied from the synchronizing signal separating circuit 822.

The data selector 824 separates the transmission data into the n-bit data D_{max} and D_{min} and the k-bit codes $\Delta_{i,j}$ quantized between the values D_{max} and D_{min}. These separated data are supplied to serial-to-parallel (S-P) converters 825 and 825', respectively, and are converted into parallel data thereby. The MAX and MIN value data D_{max} and D_{min} converted into the parallel data by the S-P converter 825 are latched by latch circuits 826 and 827, respectively. The latched MAX and MIN value data D_{max} and D_{min} are supplied to a divided value inverting circuit 828. The division code $\Delta_{i,j}$ associated with all the pixel data in each pixel block are output from the S-P converter 825' in a predetermined order and are supplied to the divided value inverting converter 828.

Fig. 4B is a view showing a state wherein representation data $D_{i,j}'$ associated with the original pixel data are decoded from the division code $\Delta_{i,j}$ and the MAX and MIN value data D_{max} and D_{min}. As shown in Fig. 4B, the representation value is set to be an intermediate value between the adjacent ones of 2^k quantization levels between the values D_{max} and D_{min}. The resultant n-bit representation value data ($D_{1,1}'$ to $D_{m,t}'$) from the divided value inverting circuit 828 are output in units of pixel blocks in the predetermined order. In a scan convert circuit 829, output data from the divided value inverting circuit 828 is converted in an order corresponding to raster scan, and the obtained data appears as decoded image data at an output terminal 830.

In the conventional arrangement, however, in order to correct a data error occurring on the transmission line, the error correction code must be added to the transmission data at the transmitting side, and the obtained data is sent onto the transmission line. At the receiving side, the data error occurring on the transmission line is corrected by using the error correction code. Redundancy of the transmission data is increased by the error correction code, and transmission efficiency cannot be improved much.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image information transmitting system which can solve the conventional problems described above.

It is another object of the present invention to provide an image information transmitting method which can effectively transmit high-quality image information.

In order to achieve this object according to an aspect of the present invention, there is provided a method of transmitting image information, comprising:

the first step of dividing a plurality of pixel data constituting one frame into a plurality of pixel data blocks for every predetermined number of pixel data;

the second step of forming distribution information data representing a distribution of values of the pixel data constituting each pixel data block in units of the plurality of pixel data blocks divided by the first step and position information data representing a correspondence between the pixel data constituting the pixel data blocks and positions in the distribution of the pixel data values represented by the distribution information data, and of transmitting the distribution information data and the position information data onto a transmission line; and

the third step of receiving the distribution information data and the position information data sent onto the transmission line and interpolating data having an error in the transmitted data by interpolation data.

It is still another object of the present invention to provide an image information transmitting system which can efficiently transmit high-quality image information.

In order to achieve the above object according to another aspect of the present invention, there is provided an image information transmitting system comprising:

pixel data block forming means of inputting an image information signal constituted by a plurality of pixel data which forms one frame, and forming a plurality of pixel data blocks from the input image information signal, each of the plurality of pixel data blocks being formed by a predetermined number of pixel data;

transmitting means for forming dynamic range in-

formation data associated with a dynamic range of values of the pixel data constituting each pixel data block in units of the plurality of pixel data blocks formed by the pixel data block forming means, coding the pixel data constituting the pixel data block by using the dynamic range information data, forming a plurality of coded data in units of pixel data blocks, and transmitting the dynamic range information data and the coded data onto a transmission line; and

interpolating means for receiving the dynamic information data and the coded data transmitted onto the transmission line by the transmitting means and interpolating data having an error in the dynamic range information data and the coded data by interpolation data.

The above and other objects, features, and advantages of the present invention will be apparent from the detailed description of the preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram of a transmitting side in a conventional image information transmitting system;

Fig. 2 is a view showing a state wherein all pixel data are divided into pixel blocks;

Fig. 3 is a view showing data layout of each pixel block;

Fig. 4A is a view showing conversion characteristics of a divided value converting circuit shown in Fig. 1;

Fig. 4B is a view showing conversion characteristics of a divided value inverting circuit shown in Fig. 6 (to be described later);

Fig. 5A is a view showing a data string output from a data selector 308 shown in Fig. 1;

Fig. 5B is a view showing a transmission data string output from the transmitting system shown in Fig. 1;

Fig. 6 is a schematic block diagram of a receiving side corresponding to the transmitting side of the image information transmitting system shown in Fig. 1;

Fig. 7A is a schematic block diagram of a transmitting side of an image information transmitting system according to the first embodiment of the present invention;

Fig. 7B is a view showing a transmission data string output from the transmitting side shown in Fig. 7A;

Fig. 8 is a schematic block diagram of a receiving side of the image information transmitting system according to the first embodiment of to the present invention;

Fig. 9A is a schematic block diagram of a transmitting side of an image information transmitting system according to the second embodiment of the present invention;

Fig. 9B is a view showing a transmission data string output from the transmitting side shown in Fig. 9A;

Fig. 10 is a schematic block diagram of a receiving side of the image information transmitting system according to the second embodiment of the present invention;

Fig. 11A is a schematic block diagram of a transmitting side of an image information transmitting system according to the third embodiment of the present invention;

Fig. 11B is a view showing a transmission data string output from the transmitting side shown in Fig. 11A; and

Fig. 12 is a schematic block diagram of a receiving side of the image information transmitting system according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described in detail with reference to the preferred embodiments hereinafter.

Fig. 7A shows a schematic arrangement of a transmitting side of an image information transmitting system according to the first embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 7A, and a detailed description thereof will be omitted.

In this transmitting side shown in Fig. 7A, unlike the transmitting side shown in Fig. 1, an error detection code adding circuit 101 adds q- and r-bit error detection codes to serial data output from a data selector 308a, and the obtained data are supplied to a FIFO memory 310, as shown in Fig. 7B.

With the above arrangement, the error detection codes added by the error detection code adding circuit 101 are used to detect whether an error occurs in data. The number of bits of the error detection codes can be smaller than that of the error correction code, and redundancy of the transmission data can be reduced.

Fig. 8 shows a schematic arrangement of a receiving side of the image information transmitting system according to the first embodiment of the present invention.

Referring to Fig. 8, the receiving side includes an input terminal 201 for receiving transmission data (Fig. 7B) coded with high efficiency by the transmitting side of Fig. 7A. The input transmission data is supplied to a data selector 202, an error detection circuit 203, and a synchronizing signal

separating circuit 204.

In the synchronizing signal separating circuit 204, a synchronizing signal is separated from the input transmission data, and the separated synchronizing signal is supplied to the error detection circuit 203 and a timing control circuit 205.

The timing control circuit 205 controls operation timings of the respective circuits in the receiving side on the basis of the synchronizing signal supplied from the synchronizing signal separating circuit 204. The data selector 202 supplies the n-bit data D_{max} to the A side, the n-bit data D_{min} to the B side, and the k-bit code $\Delta_{i,j}$ obtained by quantizing the data between the data D_{max} and D_{min} to the C side. These data are converted by serial-to-parallel (S-P) converters 206a, 206b, and 206c into parallel data, respectively.

The MAX value data D_{max} of each pixel block which is converted into the parallel data by the S-P converter 206a is supplied to a memory 207a, the B terminal of a data selector 208a, and an operation circuit 209a. The MIN value data D_{min} of each pixel block which is converted into the parallel data by the S-P converter 206b is supplied to a memory 207b, the B terminal of a data selector 208b, and an operation circuit 209b. The division code $\Delta_{i,j}$ associated with each pixel data within each pixel block and converted into the parallel data by the S-P converter 206c is supplied to a memory 207c, the B terminal of a data selector 208c, and a MAX value latch 210.

The memories 207a, 207b, and 207c are used to delay the input data by a one-field period each. The A terminals of the data selectors 208a, 208b, and 208c receive the MAX value data D_{max}, the MIN value data D_{min}, and the division code $\Delta_{i,j}$, respectively, of the immediately preceding field period.

Of the division codes $\Delta_{i,j}$ associated with the pixel data within each pixel block output and output from the S-P converter 206c, division data representing a maximum value is latched by the latch 210. The division data latched by the MAX value latch 210 is supplied to the operation circuits 209a and 209b. The operation circuit 209a calculates interpolation MIN data D_{min}' by using the MAX value data D_{max} supplied from the S-P converter 206a and the division data supplied from the MAX value latch 210. The interpolation MIN value data D_{min}' is supplied to the C terminal of the data selector 208b. The operation circuit 209b calculates interpolation MAX value data D_{max}' by using the MIN value data D_{min} supplied from the S-P converter 206b and the division data supplied from the MAX value latch 210. The interpolation MAX value data D_{max}' is supplied to the C terminal of the data selector 208a.

Note that switching of the data selectors 208a, 208b, and 208c is controlled by an error detection result output from the error detection circuit 203. More specifically, when the error detection circuit 203 detects that no error occurs in the transmission data, the data selectors 208a to 208c are connected to the corresponding B terminals. When only the MAX value data D_{max} has an error, the data selector 208a is connected to the C terminal, and the data selectors 208b and 208c are connected to the B terminals, respectively. When only the MIN value data D_{min} has an error, the data selector 208b is connected to the C terminal, and the data selectors 208a and 208c are connected to the B terminals, respectively. When both the MAX and MIN value data D_{max} and D_{min} have errors, the data selectors 208a and 208b are connected to the A terminals, respectively, and the data selector 208c is connected to the B terminal. When the division code $\Delta_{i,j}$ has an error, all the data selectors 208a to 208c are connected to the A side.

In the above operation, when an error occurs in the transmission data, the interpolation data is output from the data selector 208a, the data selector 208b, and/or the data selector 208c. The MAX value data D_{max}, the MIN value data D_{min}, and the division code $\Delta_{i,j}$ respectively output from the data selectors 208a, 208b, and 208c are supplied to a divided value inverting circuit 211. The divided value inverting circuit 211 decodes the n-bit representation data $D_{i,j}$ associated with the original pixel data on the basis of the division code $\Delta_{i,j}$ and the data D_{max} and D_{min} as in the receiving side shown in Fig. 6. The decoded data is supplied to a scan convert circuit 212. The scan convert circuit 212 converts the output data from the divided value inverting circuit 211 in an order corresponding to raster scan, and the converted data is output as decoded image data from an output terminal 213.

As described above, even if data having high redundancy such as an error correction code need not be added to image data during its transmission, the image data can be transmitted without its degradation.

In this embodiment, when an error occurs in the MAX value data D_{max}, the MIN value data D_{min}, and/or the division code $\Delta_{i,j}$ in the transmission data, the transmission data of an immediately preceding field period stored in the memories 207a, 207b, and 207c can be transmitted to the divided value inverting circuit 211 as interpolation data in place of the data having the error. However, the present invention is not limited to this scheme. For example, the transmission data of an immediately preceding field period, of transmission data which corresponds to an error, and transmission data corresponding to neighboring pixel blocks of a pixel block represented by the transmission data of the immediately preceding field period may be

used to calculate interpolation data. With this arrangement, degradation of the image data can be minimized.

As described above, according to this embodiment, there is provided a method and system for efficiently transmitting high-quality image information.

The second embodiment of the present invention will be described below.

Fig. 9A shows a schematic arrangement of a transmitting side of an image information transmitting system according to the second embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 9A, and a detailed description thereof will be omitted.

In this transmitting side shown in Fig. 9A, unlike the transmitting side shown in Fig. 1, an error detection code adding circuit 101 adds q- and r-bit error detection codes to serial data output from a data selector 308a, and the obtained data are supplied to a FIFO memory 310, as shown in Fig. 9B.

With the above arrangement, the error detection codes added by the error detection code adding circuit 101 are used to detect whether an error occurs in data. The number of bits of the error detection codes can be smaller than that of the error correction code, and redundancy of the transmission data can be reduced.

Fig. 10 shows a schematic arrangement of a receiving side of the image information transmitting system according to the second embodiment of the present invention.

Referring to Fig. 10, the receiving side includes an input terminal 1201 for receiving transmission data (Fig. 9B) coded with high efficiency by the transmitting side of Fig. 9A. The input transmission data is supplied to memories 1202 and 1203, an error detection circuit 1204, and a synchronizing signal separating circuit 1205.

The synchronizing signal separating circuit 1205 separates a synchronizing signal from the input transmission data and supplies the synchronizing signal to the error detection circuit 1204 and a timing control circuit 1217.

The timing control circuit 1217 controls operation timings of the respective circuits on the receiving side on the basis of the synchronizing signal supplied from the synchronizing signal separating circuit 1205.

The transmission data input from the input terminal 1201 are sequentially stored in the memories 1202 and 1203. The error detection circuit 1204 outputs error detection data representing that one of MAX value data D_{max}, MIN value data D_{min}, and a division code $\Delta_{i,j}$ in the transmission data input from the input terminal 1201 has an error. The error detection data output from the error detection circuit 1204 is stored in an error detection data memory 1206.

As described above, the transmission data corresponding to one-field image data is stored in the memories 1202 and 1203, and the error detection data corresponding to this transmission data is stored in the error detection data memory 1206. The data stored in the respective memories are then read out. During read access of each memory, new input transmission data and new error detection data are stored in the corresponding memory. Therefore, the memories store the new data in place of the readout data.

The transmission data stored in the memory 1203 is read out in a FIFO order and supplied to the B terminal of a data selector 1207.

When the MAX value data D_{max} or the MIN value data D_{min} has an error, an address generating circuit 1208 outputs to the memory 1202 an address for reading out the data D_{max} or D_{min} in the transmission data corresponding to the neighboring pixel blocks on the screen in response to the error detection data supplied from the error detection data memory 1206. When the division code $\Delta_{i,j}$ has an error, the address generating circuit 1208 outputs to the memory 1202 an address for reading out the codes $\Delta_{i,j}$ corresponding to the neighboring pixels in the pixel block. The stored data are read out from the memory 1202 in response to the read address output from the address generating circuit 1208. The readout data is supplied to an operation circuit 1209.

The operation circuit 1209 calculates interpolation MAX value data D_{max}', interpolation MIN value data D_{min}', and an interpolation division code $\Delta_{i,j}'$ by using the data supplied from the memory 1202. The calculated data are supplied to the A terminal of the data selector 1207.

The error detection data read out from the error detection data memory 1206 is also supplied to a data selector control circuit 1210. When a data error is represented by the input error detection data, the data selector control circuit 1210 connects the data selector 1207 to the A terminal. Otherwise, the data selector control circuit 1210 connects the data selector 1207 to the B terminal. When an error is present in the transmission data read out from the memory 1203, the data having an error is replaced with the corresponding interpolation data, and the interpolated data is output.

The transmission data output from the data selector 1207 is separated into n-bit data D_{max} and D_{min} and the division code $\Delta_{i,j}$ by a data selector 1211. These separated data are converted into parallel data by serial-to-parallel (S-P) converters 1212 and 1213.

The parallel MAX and MIN value data D_{max} and D_{min} from the S-P converter 1212 are latched by

latches 1214 and 1215, respectively. The latched MAX and MIN value data D_{max} and D_{min} are supplied to a divided value inverting circuit 1216.

The division code $\Delta_{i,j}$ converted as parallel data by the S-P converter 1213 is also supplied to the divided value inverting circuit 1216.

The divided value inverting circuit 1216 decodes n-bit representation data $D_{i,j}$ associated with the original pixel data on the basis of the division code $\Delta_{i,j}$ and the data D_{max} and D_{min} as in the receiving side shown in Fig. 6. The decoded value is supplied to a scan convert circuit 1218. The scan convert circuit 1218 converts the output data from the divided value inverting circuit 1216 in an order corresponding to raster scan. The converted data is output as decoded image data from an output terminal 1219.

As described above, without adding data having high redundancy such as an error correction code to image signal during its transmission, the image data can be corrected to an extent that image quality degradation occurring on the transmission line is negligible. Since extra data is not transmitted, transmission efficiency can be improved.

As described above, according to this embodiment, there is provided a method and system for efficiently transmitting high-quality image information.

The third embodiment of the present invention will be described below.

Fig. 11A shows a schematic arrangement of a transmitting side of an image information transmitting system according to the third embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 11A, and a detailed description thereof will be omitted.

In this transmitting side shown in Fig. 11A, unlike the transmitting side shown in Fig. 1, an error detection code adding circuit 101 adds q- and r-bit error detection codes to serial data output from a data selector 308a, and the obtained data are supplied to a FIFO memory 310, as shown in Fig. 11B.

With the above arrangement, the error detection codes added by the error detection code adding circuit 101 are used to detect whether an error occurs in data. The number of bits of the error detection codes can be smaller than that of the error correction code, and redundancy of the transmission data can be reduced.

Fig. 12 shows a schematic arrangement of a receiving side of the image information transmitting system according to the third embodiment of the present invention.

Referring to Fig. 12, the receiving side includes an input terminal 2201 for receiving transmission data (Fig. 11B) coded with high efficiency by the transmitting side of Fig. 11A. The input transmission data is supplied to a data selector 2202, an error detection circuit 2203, and a synchronizing signal separating circuit 2204.

In the synchronizing signal separating circuit 2204, a synchronizing signal is separated from the input transmission data, and the separated synchronizing signal is supplied to the error detection circuit 2203 and a timing control circuit 2205.

The timing control circuit 2205 controls operation timings of the respective circuits in the receiving side on the basis of the synchronizing signal supplied from the synchronizing signal separating circuit 2204. The data selector 2202 supplies the n-bit data D_{max} to the A side, the n-bit data D_{min} to the B side, and the k-bit code $\Delta_{i,j}$ obtained by quantizing the data between the data D_{max} and D_{min} to the C side. These data are converted by serial-to-parallel (S-P) converters 2206a, 2206b, and 2206c into parallel data, respectively.

The MAX value data D_{max} of each pixel block which is converted into the parallel data by the S-P converter 2206a is supplied to a memory 2207a and the B terminal of a data selector 2208a. The MIN value data D_{min} of each pixel block which is converted into the parallel data by the S-P converter 2208b is supplied to a memory 2207b and the B terminal of a data selector 2208b. The division code $\Delta_{i,j}$ associated with each pixel data within each pixel block and converted into the parallel data by the S-P converter 2206c is supplied to a memory 2207c, the B terminal of a data selector 2208c, and an operation circuit 2209.

The memories 2207a, 2207b, and 2207c are used to delay the input data by a one-field period each. The A terminals of the data selectors 2208a, 2208b, and 2208c receive the MAX value data D_{max}, the MIN value data D_{min}, and the division code $\Delta_{i,j}$, respectively.

The operation circuit 2209 is a circuit for calculating an average value of the division codes $\Delta_{i,j}$ associated with the pixel data of the pixel blocks output from the S-P converter 2206c. The data calculated by the operation circuit 2209 is supplied to the C terminal of the data selector 2208c, and a fixed data generator 2210 generates data representing an intermediate value of the values represented by the division codes $\Delta_{i,j}$. The output from the fixed data generator 2210 is supplied to the D terminal of the data selector 2208c.

Note that switching of the data selectors 2208a, 2208b, and 2208c is controlled by an error detection result output from the error detection circuit 2203. More specifically, when the error detection circuit 2203 detects that no error occurs in the transmission data, the data selectors 2208a to 2208c are connected to the corresponding B terminals. When only the MAX value data D_{max} has an

error, the data selector 2208a is connected to the A terminal. When only the MIN value data D_{min} has an error, the data selector 2208b is connected to the A terminal. When the MIN and MIN value data D_{max} and D_{min} and the division code $\Delta_{i,j}$ have errors, all the data selectors 2208a to 2208c are connected to the A side.

In this embodiment, when no error is present in the MAX data D_{max} and the MIN value data D_{min}, and an error is present in the division code $\Delta_{i,j}$, the data selector 2208c is connected to the C or D terminal in accordance with an error rate. More specifically, when the error detection circuit 2203 detects that the number of errors in the division codes $\Delta_{i,j}$ exceeds a predetermined number, the average value of the division codes $\Delta_{i,j}$ cannot be calculated. In this case, the data selector 2208c is connected to the D terminal, and data representing an intermediate value of the values of the division codes $\Delta_{i,j}$ is output from the data selector 2208c in place of the data representing the average value. However, when the error detection circuit 2203 detects that the detected number of errors in the division codes $\Delta_{i,j}$ is smaller than the predetermined number, the data selector 2208c is connected to the C terminal. Data representing the average value of the division codes $\Delta_{i,j}$ and calculated by the operation circuit 2209 is output from the data selector 2208c.

In the above operation, when an error occurs in the transmission data, the data selectors 2208a, 2208b, and 2208c output the corresponding interpolation data in place of the error data. The MAX value data D_{max}, the MIN value data D_{min}, and the division code $\Delta_{i,j}$ respectively output from the data selectors 2208a, 2208b, and 2208c are supplied to a divided value inverting circuit 2211. The divided value inverting circuit 2211 decodes n-bit representation value data $D_{i,j}$ associated from the original pixel data on the basis of the division code $\Delta_{i,j}$ and the data D_{max} and D_{min} as in the receiving side shown in Fig. 6. The decoded data is supplied to a scan convert circuit 2212.

The scan convert circuit 2211 converts the output data from the divided value inverting circuit 2211 in an order corresponding to raster scan. The converted data is output as decoded image data from an output terminal 2213.

As described above, even if data having high redundancy such as an error correction code is not added to image data during its transmission, various types of interpolation data can be formed in accordance with the error rate of the image data, and the data having an error is interpolated with the interpolation data. Therefore, the image data can be transmitted without being degraded.

As described above, according to this embodiment, there is provided a method and system for efficiently transmitting high-quality image information.

Claims

1. A method of transmitting image information, comprising:

(A) the first step of dividing a plurality of pixel data constituting one frame into a plurality of pixel data blocks for every predetermined number of pixel data;

(B) the second step of forming distribution information data representing a distribution of values of the pixel data constituting each pixel data block in units of the plurality of pixel data blocks divided by the first step and position information data representing a correspondence between the pixel data constituting the pixel data blocks and positions in the distribution of the pixel data values represented by the distribution information data, and of transmitting the distribution information data and the position information data onto a transmission line; and

(C) the third step of receiving the distribution information data and the position information data sent onto the transmission line and interpolating data having an error in the transmitted data by interpolation data.

2. A method according to claim 1, wherein the third step comprises the step of receiving the distribution information data and the position information data sent onto the transmission line in the second step, and interpolating the data having the error with the interpolation data formed by using already transmitted data.

3. A method according to claim 1, wherein the third step comprises the step of receiving the distribution information data and the position information data sent onto the transmission line in the second step, and interpolating the data having the error with interpolation data formed by using data which does not have an error and corresponds to the same frame as that of the data having the error.

4. A method according to claim 1, wherein the third step comprises the step of receiving the distribution information data and the position information data sent onto the transmission line in the second step, and interpolating the position information data having an error with interpolation data representing a predetermined value when no error is present in the distribution information data of the transmission data and the number of errors of the position information data exceeds a predetermined number.

5. A method according to claim 1, wherein the distribution information data are data representing maximum and minimum values of values of the

pixel data constituting the pixel data block.

6. A method according to claim 1, wherein the distribution information data are data representing a maximum value and a dynamic range of values of the pixel data constituting the pixel block.

7. A method according to claim 1, wherein the distribution information data are data representing a minimum value and a dynamic range of values of the pixel data constituting the pixel block.

8. An apparatus for transmitting image information comprising:

(A) pixel data block forming means of inputting an image information signal constituted by a plurality of pixel data which forms one frame, and forming a plurality of pixel data blocks from the input image information signal, each of the plurality of pixel data blocks being formed by a predetermined number of pixel data;

(B) transmitting means for forming dynamic range information data associated with a dynamic range of values of the pixel data constituting each pixel data block in units of the plurality of pixel data blocks formed by said pixel data block forming means, coding the pixel data constituting the pixel data block by using the dynamic range information data, forming a plurality of coded data in units of pixel data blocks, and transmitting the dynamic range information data and the coded data onto a transmission line; and

(C) interpolating means for receiving the dynamic information data and the coded data transmitted onto said transmission line by said transmitting means and interpolating data having an error in the dynamic range information data and the coded data by interpolation data.

9. An apparatus according to claim 8, wherein said interpolating means is arranged to receive the dynamic range information data and the coded data sent onto the transmission line by said transmitting means, and interpolate the data having the error with the interpolation data formed by using already transmitted data.

10. An apparatus according to claim 8, wherein said interpolating means is arranged to receive the dynamic range information data and the coded data sent onto the transmission line by the transmitting means, and interpolate the data having the error with interpolation data formed by using data which does not have an error and corresponds to the same frame as that of the data having the error.

11. An apparatus according to claim 8, wherein said interpolating means is arranged to receive the dynamic range information data and the coded data sent onto the transmission line in the second step, and interpolate the coded data having an error with interpolation data representing a predetermined value when no error is present in the dynamic range information data of the transmission data and the number of errors of the coded data exceeds a predetermined number.

12. An apparatus according to claim 11, wherein the interpolation data is coded data corresponding to an intermediate value in the dynamic range represented by the dynamic range information data.

13. An apparatus according to claim 8, wherein the dynamic range information data are data representing maximum and minimum values of values of the pixel data constituting the pixel data block.

14. An apparatus according to claim 8, wherein the dynamic range information data are data representing a maximum value and a dynamic range of values of the pixel data constituting the pixel block.

15. An apparatus according to claim 8, wherein the dynamic range information data are data representing a minimum value and a dynamic range of values of the pixel data constituting the pixel block.

16. A method of transmitting image data in which the data is divided into blocks, data is transmitted for a said block, the transmitted data comprising: data relating to the range of values of the image data in the block; and image data in the block compressed in Occordance with the said range of values, and the transmitted data is received and image data for the block is derived from it,
characterised in that
if an error is detected in the received data, the detected erroneous data is replaced by substitute data.

17. A method according to claim 16 in which the substitute data is derived by interpolation.

18. A method according to claim 16 in which the substitute data is copied from previously transmitted data.

19. A method according to any one of claims 16 to 18 in which the substitute data is derived using data from a previous block.

20. A method according to any one of claims 16 to 19 in which the image data has fields, and the substitute data is derived using data from a previous field.

21. A method according to any one of claims 16 to 20 in which the transmitted data is coded for error detection but not for error correction.

22. Data receiving apparatus for receiving data and substituting detected erroneous data by a method according to any one of claims 16 to 21.

FIG. 1

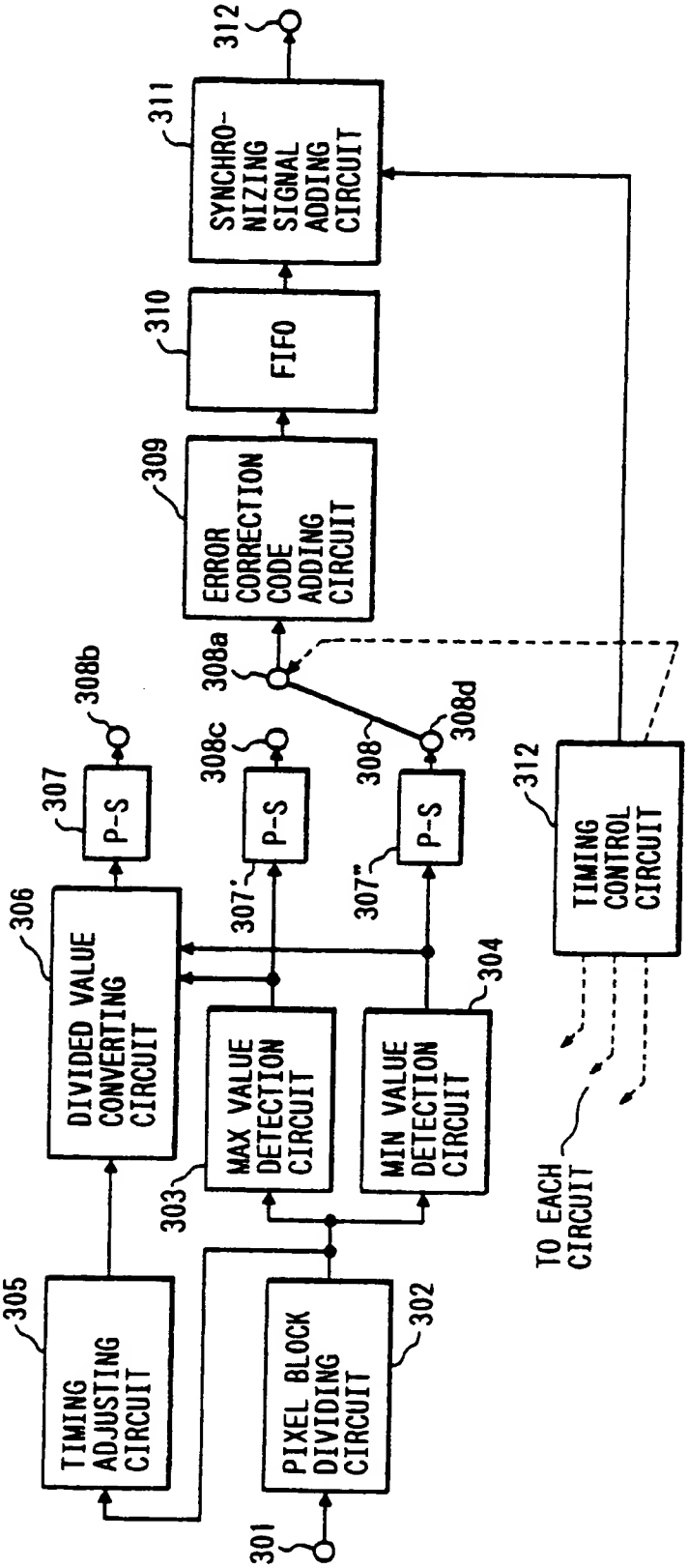

301
PIXEL BLOCK DIVIDING CIRCUIT
302
TIMING ADJUSTING CIRCUIT
305
DIVIDED VALUE CONVERTING CIRCUIT
306
MAX VALUE DETECTION CIRCUIT
303
MIN VALUE DETECTION CIRCUIT
304
P-S
307
307'
307"
308
308a
308b
308c
308d
ERROR CORRECTION CODE ADDING CIRCUIT
309
FIFO
310
SYNCHRO-NIZING SIGNAL ADDING CIRCUIT
311
312
TIMING CONTROL CIRCUIT
TO EACH CIRCUIT

FIG. 2

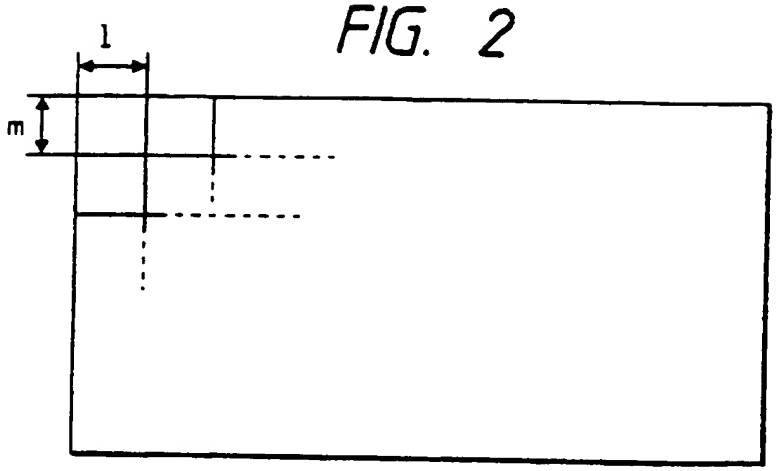


FIG. 3

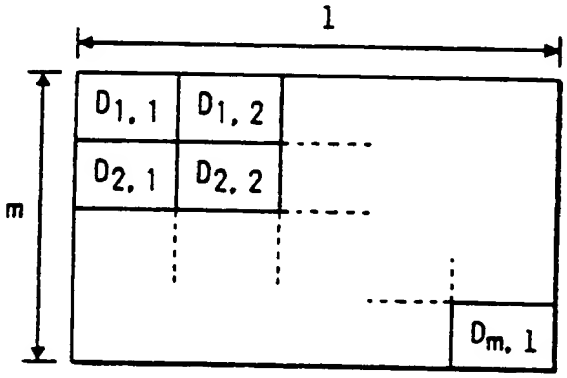


FIG. 4A

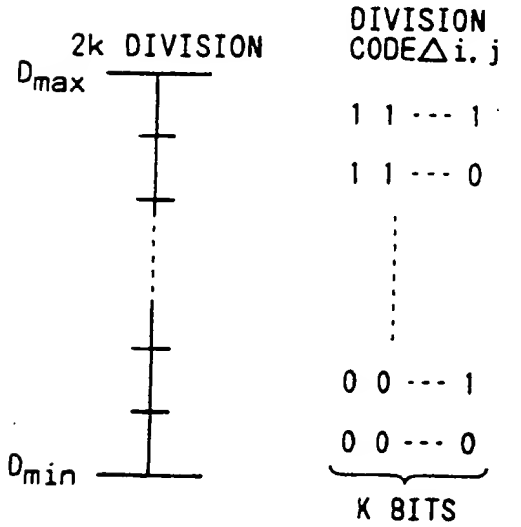


FIG. 4B

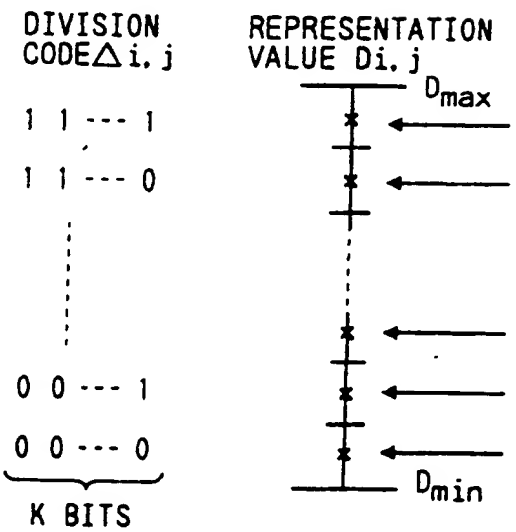


FIG. 5A

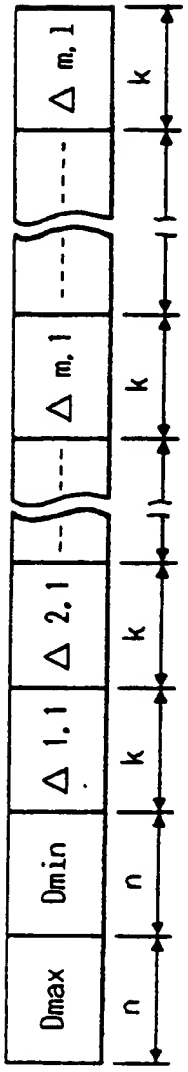


FIG. 5B

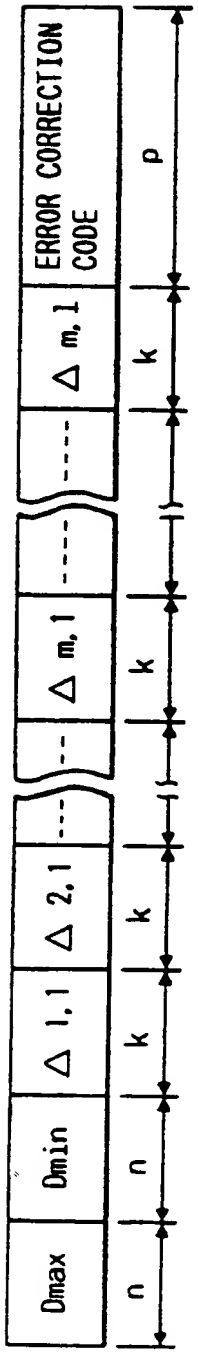


FIG. 6

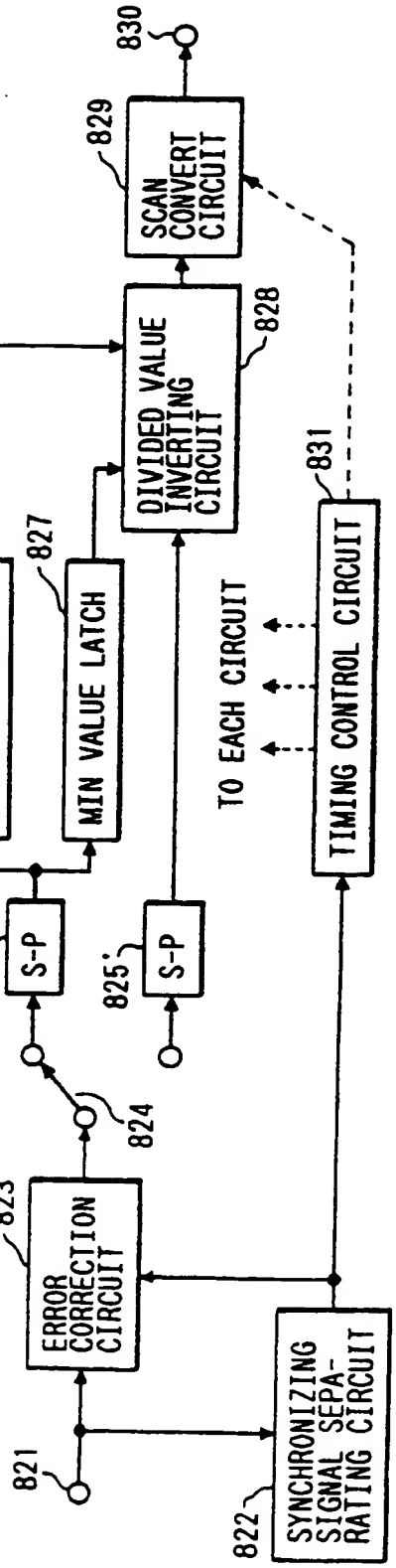


FIG. 7A

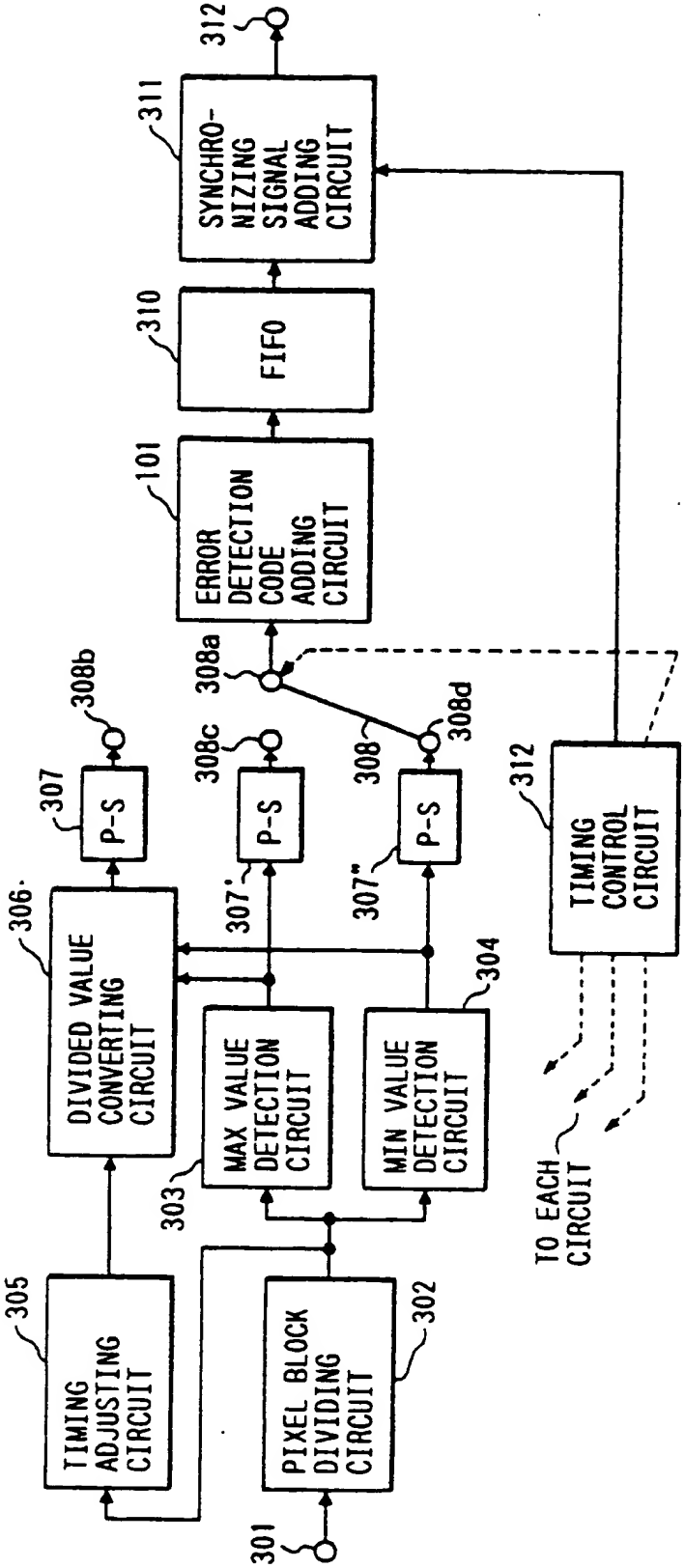

301
PIXEL BLOCK DIVIDING CIRCUIT
302
TIMING ADJUSTING CIRCUIT
305
DIVIDED VALUE CONVERTING CIRCUIT
306
MAX VALUE DETECTION CIRCUIT
303
MIN VALUE DETECTION CIRCUIT
304
P-S
307
307'
307"
308b
308c
308
308d
308a
ERROR DETECTION CODE ADDING CIRCUIT
101
FIFO
310
SYNCHRO-NIZING SIGNAL ADDING CIRCUIT
311
312
TIMING CONTROL CIRCUIT
TO EACH CIRCUIT

FIG. 7B

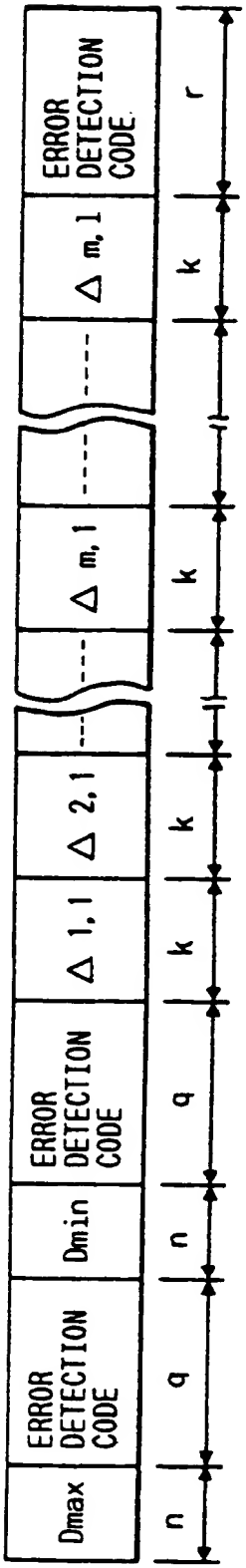

Dmax
ERROR DETECTION CODE
Dmin
ERROR DETECTION CODE
Δ 1, 1
Δ 2, 1
Δ m, 1
Δ m, 1
ERROR DETECTION CODE
n
q
n
q
k
k
k
k
r

FIG. 8

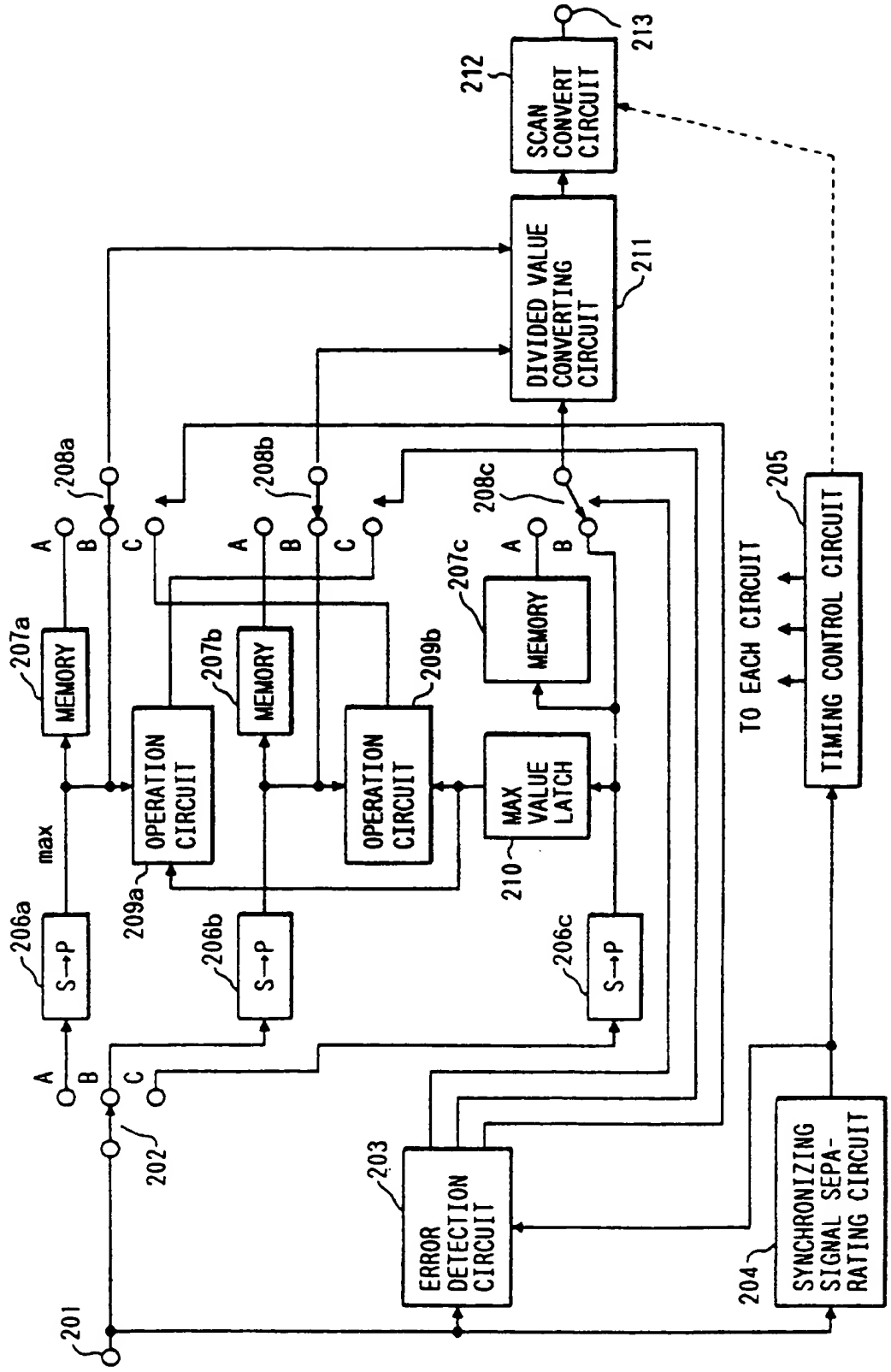

201
202
203
204
205
206a
206b
206c
207a
207b
207c
208a
208b
208c
209a
209b
210
211
212
213
A
B
C
max
S→P
MEMORY
OPERATION CIRCUIT
MAX VALUE LATCH
ERROR DETECTION CIRCUIT
SYNCHRONIZING SIGNAL SEPARATING CIRCUIT
TIMING CONTROL CIRCUIT
TO EACH CIRCUIT
DIVIDED VALUE CONVERTING CIRCUIT
SCAN CONVERT CIRCUIT

FIG. 9A

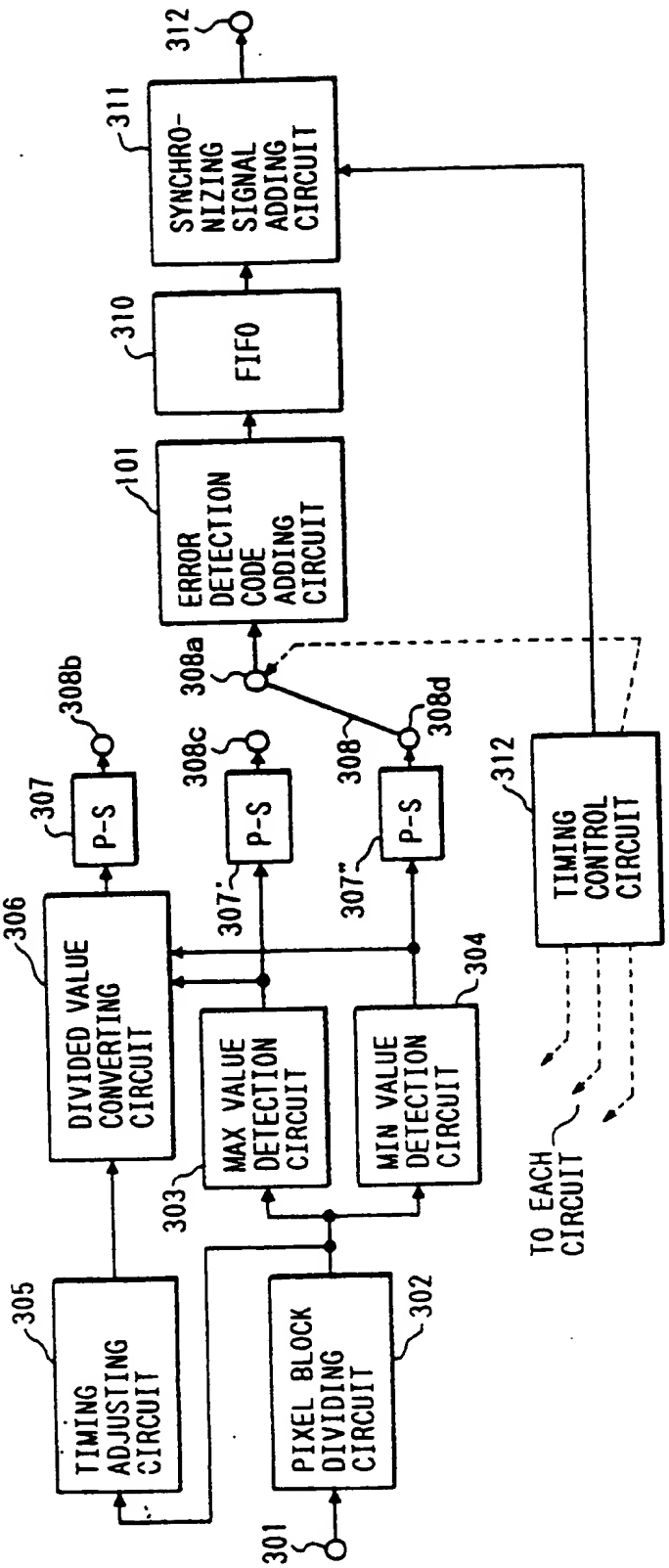

301
PIXEL BLOCK DIVIDING CIRCUIT
302
303
MAX VALUE DETECTION CIRCUIT
304
MIN VALUE DETECTION CIRCUIT
305
TIMING ADJUSTING CIRCUIT
306
DIVIDED VALUE CONVERTING CIRCUIT
307
307'
307"
P-S
308a
308b
308c
308d
308
ERROR DETECTION CODE ADDING CIRCUIT
101
FIFO
310
SYNCHRO-NIZING SIGNAL ADDING CIRCUIT
311
312
TIMING CONTROL CIRCUIT
TO EACH CIRCUIT

FIG. 9B

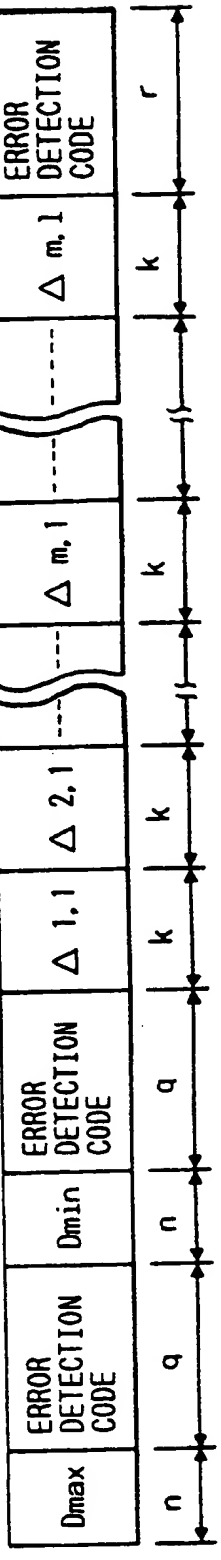

Dmax
ERROR DETECTION CODE
Dmin
ERROR DETECTION CODE
Δ 1, 1
Δ 2, 1
Δ m, 1
Δ m, 1
ERROR DETECTION CODE
n
q
n
q
k
k
k
k
k
r

FIG. 10

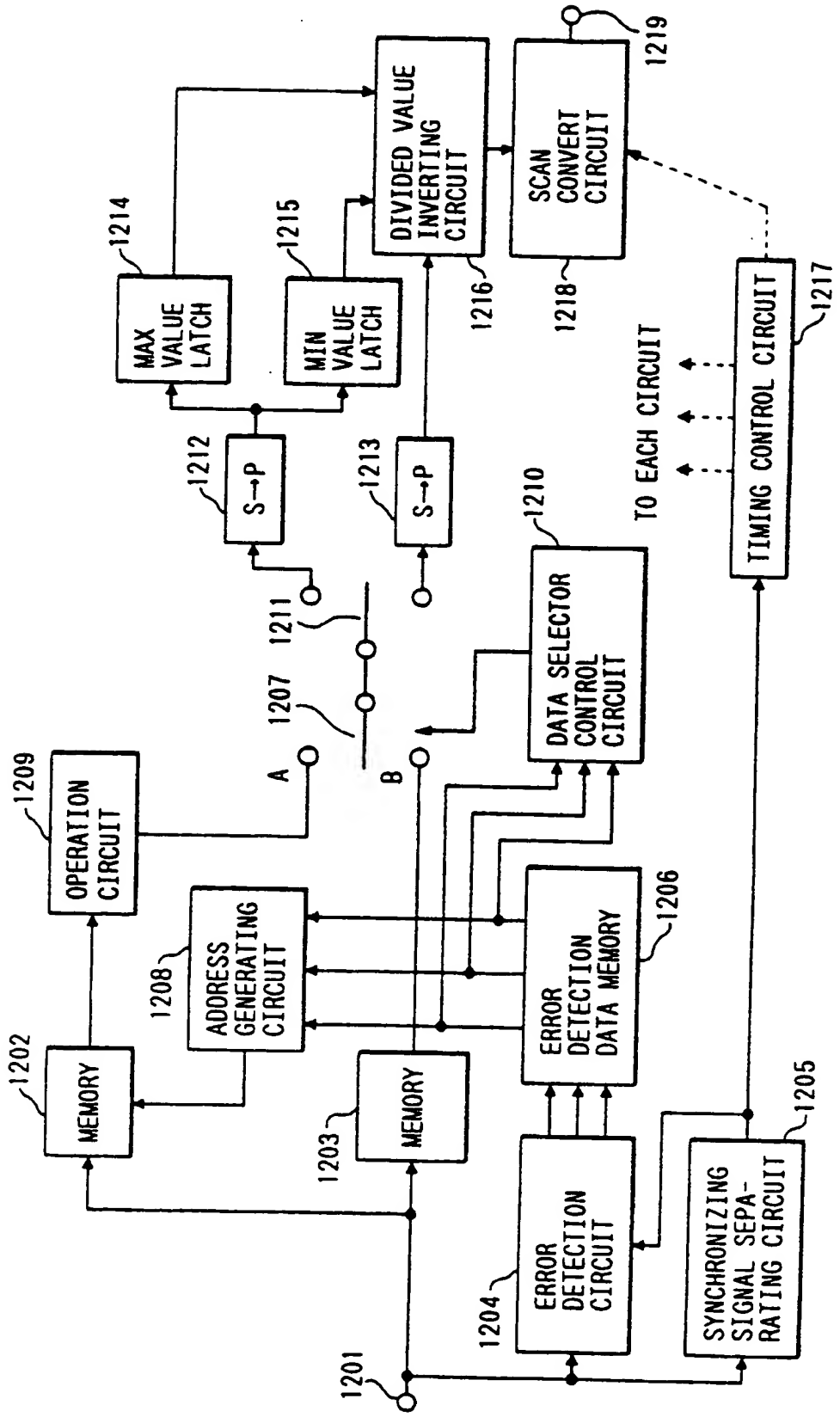

1201
1202
MEMORY
1203
MEMORY
1204
ERROR DETECTION CIRCUIT
1205
SYNCHRONIZING SIGNAL SEPARATING CIRCUIT
1206
ERROR DETECTION DATA MEMORY
1207
A
B
1208
ADDRESS GENERATING CIRCUIT
1209
OPERATION CIRCUIT
1210
DATA SELECTOR CONTROL CIRCUIT
1211
1212
S→P
1213
S→P
1214
MAX VALUE LATCH
1215
MIN VALUE LATCH
1216
DIVIDED VALUE INVERTING CIRCUIT
1217
TIMING CONTROL CIRCUIT
1218
SCAN CONVERT CIRCUIT
1219
TO EACH CIRCUIT

FIG. 11A

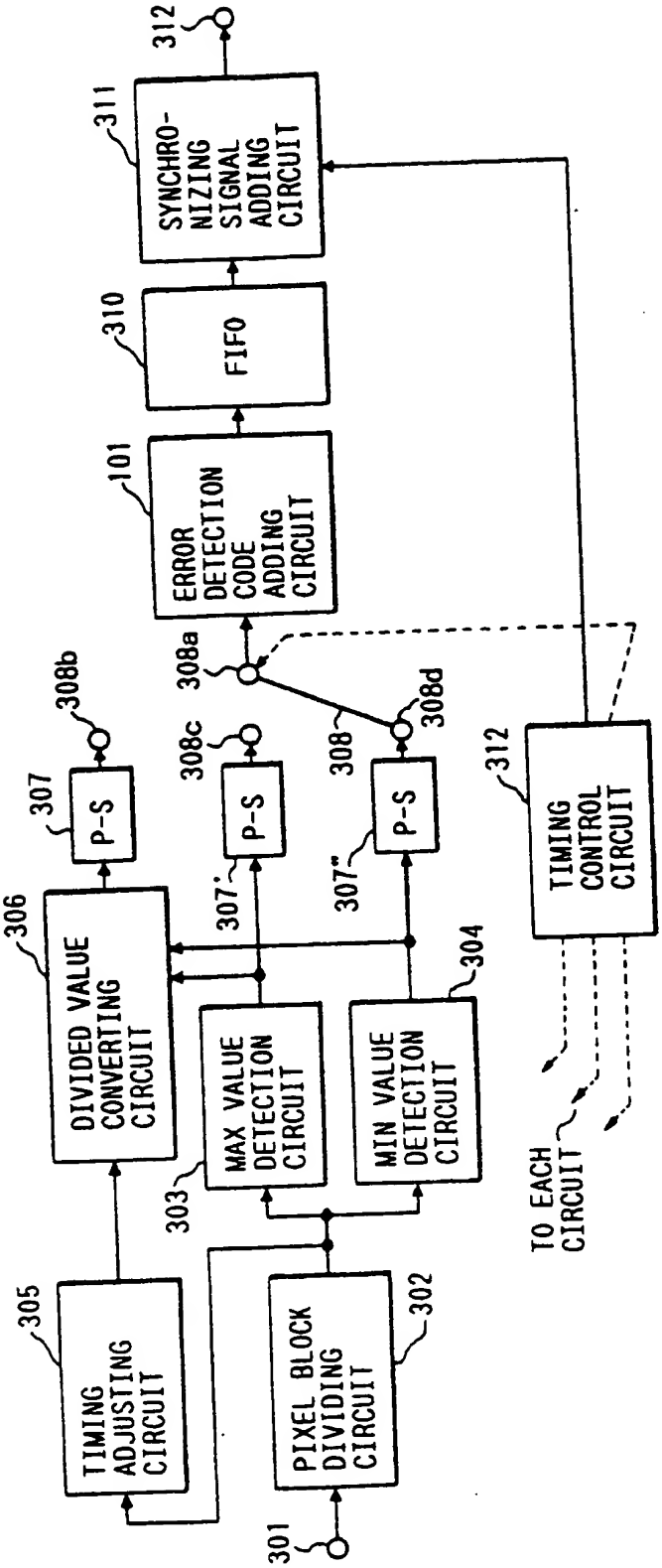


FIG. 11B

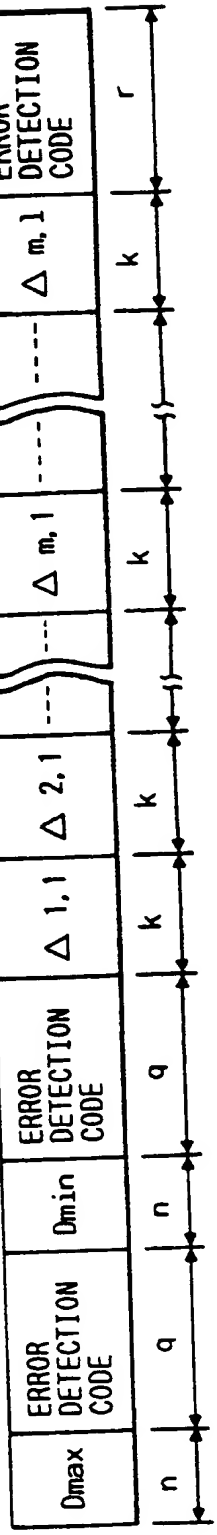
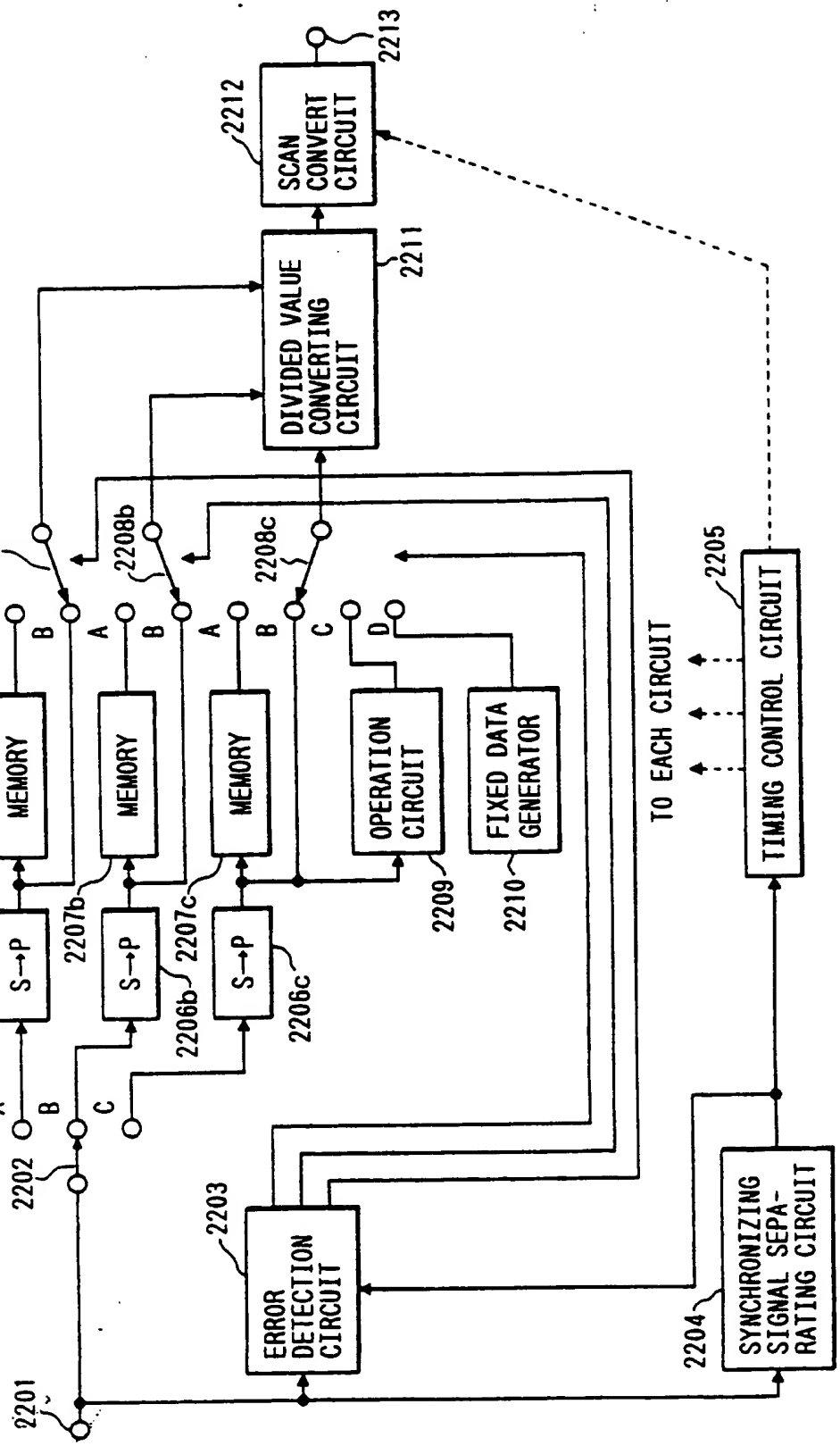


FIG. 12


2213
2212
SCAN CONVERT CIRCUIT
2211
DIVIDED VALUE CONVERTING CIRCUIT
2208a
2208b
2208c
A
B
C
D
2207a
MEMORY
2207b
2207c
OPERATION CIRCUIT
2209
FIXED DATA GENERATOR
2210
2206a
S→P
2206b
2206c
2202
2203
ERROR DETECTION CIRCUIT
2201
2204
SYNCHRONIZING SIGNAL SEPARATING CIRCUIT
2205
TIMING CONTROL CIRCUIT
TO EACH CIRCUIT